VLSI Realization of a Two-Dimensional Hamming Distance Comparator ANN for Image Processing Applications

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Abstract. This paper presents the hardware realization of a Hamming artificial neural network, and demonstrates its use in a high-speed precision alignment system. High degree of parallelism is exploited in the proposed architecture, where the result of NxN array of sum of products is provided simultaneously. The full operation of the artificial neural network requires three clock cycles, which are shown to be completed within a few tens of nanoseconds, depending on the chosen architecture, thus realizing a complex operation using a fast and low-power circuit. Possible applications of the device include industrial image processing such as focus recovery, fast and precise alignment in a noisy environment, and vehicle navigation systems.

1 Introduction

The efficient hardware integration of neural network based paradigms is a key element in speeding up the implementation of such algorithms, targeting real-time applications while taking full benefit of their inherent parallel operation mode. The focus of the work described in the following is the development and integration into an integrated circuit of a specific NN model which is shown to allow several image processing applications.

The proposed Hamming artificial neural network (ANN) performs Hamming distance calculation between a previously stored set of patterns, and the current input, based on a three layer architecture. It has the ability to classify noise corrupted patterns and always converges toward one of the stored patterns.

The input layer is considered as the first layer. The second layer, the quantifier network, is composed of a number of neurons, each of which processing the Hamming distance calculation that is to be delivered to the third layer. The third layer, the discrimination network, processes a winner-take-all (WTA) operation where the selection of the second-layer neuron with smallest Hamming distance is selected by the means of a feedback scheme.

Earlier, portions of the Hamming ANN have been successfully integrated on-chip using the capacitive mode of operation [1] as a pattern classifier. The capacitive network was implemented using the capacitive threshold logic (CTL) gate described in [2], whereas the WTA circuit was derived as multiple input adaptation of a regular sense amplifier as used in integrated memory circuits.

The use of CTL as an analog circuit technique offers several benefits with respect to standard digital CMOS circuit designs, such as low-power of operation, compact design and high-speed processing of weighted sum of very large input vectors qualifying its use in signal processing applications [3]. On the other hand, the analog WTA circuit proposed earlier is extremely dependent to the technology, i.e. the transistors have to be resized for every new design.

In this paper, we propose a novel circuit design which combines the CTL gate with an original WTA scheme increasing the information content of the output signals. Section 2 describes the physical design of the new Hamming ANN circuit and its operation. The possible working modes are described in Section 3, while the application of the circuit to the field of image processing is demonstrated in Section 4.

2 A Hamming Artificial Neural Network Architecture and Design

An adapted version of the capacitive neuron proposed in [4] was developed in order to integrate the WTA operation into the quantifier network as an extra input which is capacitively coupled to the row. The proposed circuit operates in a three cycle scheme consisting of a reset, an evaluation and a perturbation phase, each of which being driven by it own clocking signal, as depicted in Figure 1.

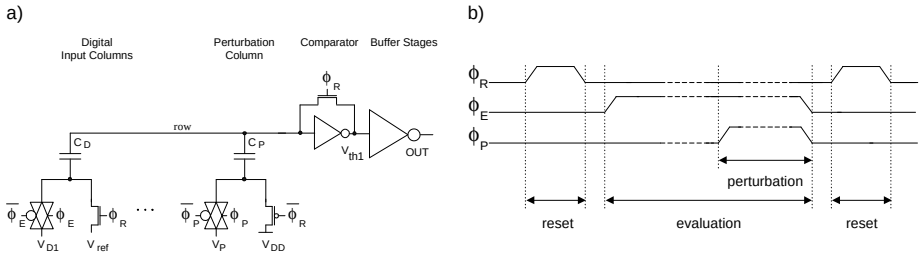

Figure 1: a) Modified CTL gate supporting analog capacitive row perturbation, and b) clocking scheme of the driving signals.

The circuit operation is based on charge conservation which applies during all three cycles. All row and column voltages are set to a reference value during the reset phase (Equation 1). The input vector is applied during the evaluation phase, thus causing a modification of the row voltage by capacitive coupling to the columns (Equation 2). The resulting row voltage is proportional to the Hamming distance of the input vector and the pattern which is stored in the form of the capacitance joining rows and columns. A binary value is produced at the output of each row's comparator stage as the as decision of the row voltage being above or below the comparator's threshold value (Equation 3). Eventually a perturbation signal is applied to one extra column called perturbation column, which causes an additional perturbation of the row voltage. The nature of the perturbation signal allows different operation modes of the circuit. Applying a descending linear ramp as a perturbation signal will cause each of the row comparator circuits to switch with a delay proportional to the Hamming distance stored in

the row voltages. This approach, combined with digital circuitry builds an adaptable k-WTA unit. Also note that the circuit operation allows subsequent processing of several input vectors in a consecutive manner, before a new reset is applied. The operation of the CTL-based Hamming network is demonstrated by SPICE simulations using a 0.35 CMOS technology, and is shown in Figure 2.

$$Q_{reset} = (V_{th1} - V_{ref})C_D^{TOT} + (V_{th1} - V_{DD})C_P \quad \text{with} \quad C_D^{TOT} = \sum_n C_{D_n} \tag{1}$$

$$Q_{eval} = \sum_n (V_{row} - V_{D_n})C_{D_n} + (V_{row} - V_P)C_P \tag{2}$$

$$\Delta V_{row} = \frac{\sum_n (V_{D_n} - V_{ref})C_D^{TOT} + (V_P - V_{DD})C_P}{C_D^{TOT} + C_P}$$

$$\begin{cases} \Delta V_{row} < 0 \Rightarrow V_{OUT} = V_{DD} \\ \Delta V_{row} > 0 \Rightarrow V_{OUT} = GND \\ \Delta V_{row} = 0 \Rightarrow \text{limit of the circuit precision} \end{cases} \tag{3}$$

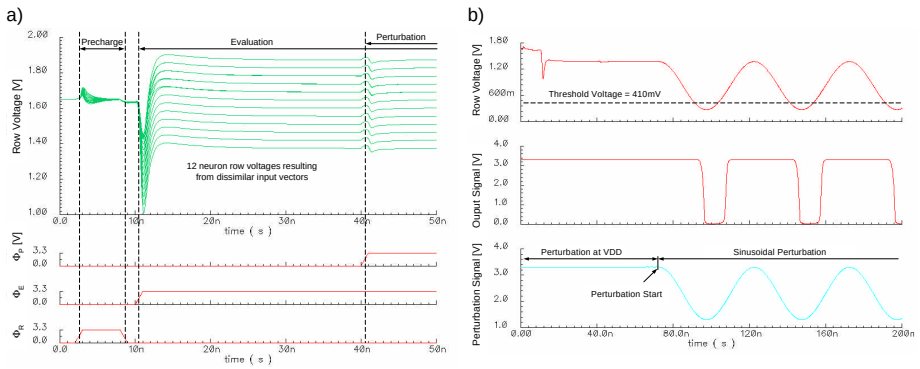

Figure 2: SPICE simulations of a) row voltage variations during regular discrimination of twelve neurons with increasing absolute input values, and b) row and output voltages of one neuron, including a sinusoidal perturbation signal.

3 Operation Modes of the Proposed Hamming ANN

Two operation modes derive immediately from the possible alternate circuit architectures based on the principle described in Section 2. Relative Hamming calculations are possible in an architecture similar as the one described in [1], where any ‘Logic 1’ is implemented as a unit capacitance and any ‘Logic 0’ is formed of a very small capac-

itance resulting from undesired lines overlap, or ideally no capacitance at all. This circuit cannot be used without any WTA, the output from the quantifier network having a meaning only relatively to the other neurons answers. The second mode of operation is associated to the circuit depicted in Figure 3 b) where the ‘Logic 1’ and ‘Logic 0’ levels are processed in the input logic access circuitry. In this case, the Hamming distance is absolute, with respect to the built-in analog voltage reference.Two alternate working

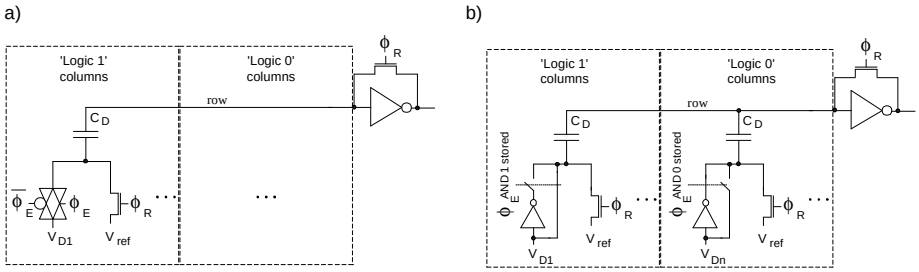

Figure 3: Circuits associated to the two possible operation modes in a) relative and b) absolute Hamming distance calculation.

modes relating to the nature of the applied perturbations can be considered. A WTA operation can be emulated by application of a ramp shape signal to the perturbation column. As presented in Figure 4 a), all evaluated row voltages follow a linear ramp caused by the pertubation. Consequently, the output signal switches when the row voltage gets lower than the comparator threshold voltage, thus delivering a ranking information related to their Hamming distance in the time domain. The ranked k-WTA operation can be processed the same way, using additional digital output circuits. Using a pulse of calibrated amplitude allows the direct synthesis of the k-WTA operation. The information provided can be described as the discrimination of the neurons which have a Hamming distance inside of a selected interval.

A number of Hamming distance based signal processing operations can be synthesized using selected working modes, also depending on the affordable cost in terms of digital output circuits, ranging from none to complex post processing units, thus allowing a wide range of applications to benefit from the alternate modes and architectures. In the following we demonstrate the proposed system in an image processing application as a case study.

4 A Precision Alignment System based on Hamming Distance Processing

Two-dimensional image processing requires an array arrangement of the CTL-based neuron, where each input is capacitively coupled to neurons which are assigned to store horizontal and vertical pixel information respectively, as shown in Figure 5.

Matlab simulations of an array based on the absolute Hamming distance neuron with ramp perturbation have demonstrated the successful use of the system in applica-

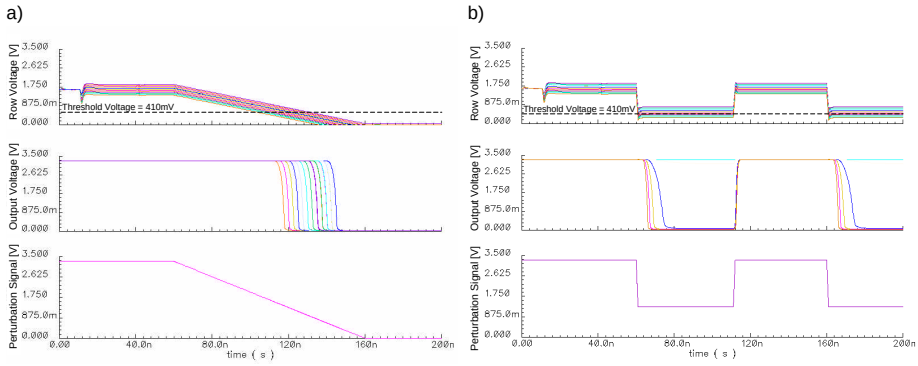

Figure 4: SPICE simulations of the circuit under two different analog perturbations: a) linear ramp perturbation, and b) controlled amplitude pulse.

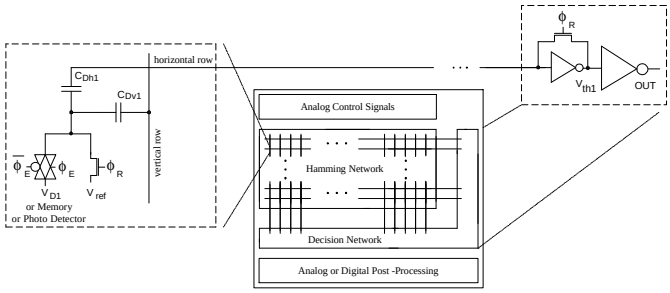

Figure 5: Array arrangement of the Hamming distance classifier.

tions requiring precision alignment features. Relatively small images of 16x16 pixels were used in order to reduce the simulation time, under the constraints of relative symmetry of the pattern which is centered, and the presence of a minimal portion of the searched pattern inside the grid. The grid is virtually divided into two equal windows, vertically and horizontally. The applied control algorithm is limited to summing the Hamming distances of each 8x16 window, then applying a correction signal corresponding to the direction pointed out as the smallest of both sums. The operation is repeated for vertical and horizontal sums. Two possible resulting correction signals were experimented with, the result of which operation can be seen on Figure 6. In the first case, the correction signal is proportional to the sums, whereas in the second case a correction corresponding to a move equal to one pixel is applied. The system proved to be able to process noisy, translated and rotated patterns.

It is important to mention that the complexity of the post-processing, may it be digital or analog, can be adapted to the required performances in terms of speed of convergence, acceptable hardware overhead. In any case, this unit can be designed as a very compact and fast unit, resulting from a limited set of required operations, namely additions, thresholding, and possibly multiplication, all of which can be advantageously processed by a CTL gate.

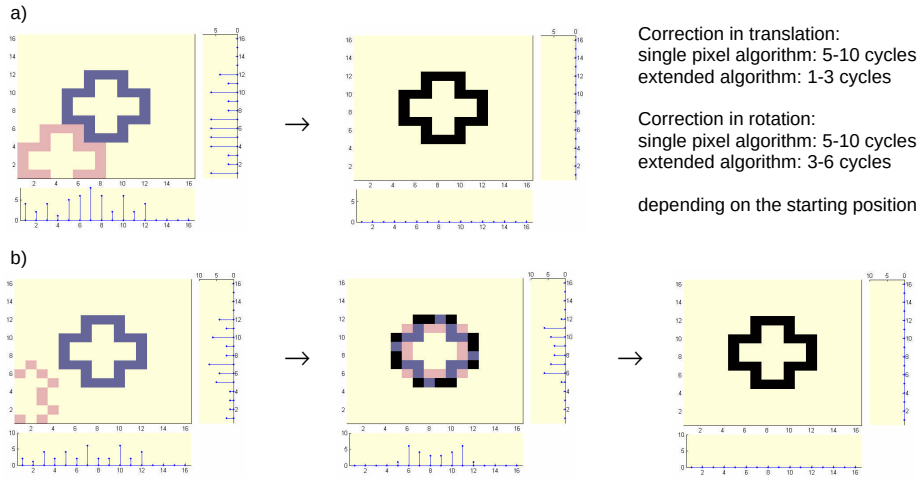

Figure 6: Matlab simulation demonstrating the convergence of the system facing a) translated and b) translated-rotated patterns. Hamming distance shown on the side diagram.

5 Conclusions

In this paper we have demonstrated the adaptation of the Hamming ANN circuit in order to support the capacitive row perturbation scheme. A novel k-WTA concept based on row perturbation, WTA discrimination in the time domain, and reduced post-processing has been proposed, which gives the circuit the ability to extract extended information content in terms of absolute and relative Hamming distances. Depending on the nature of the targeted application, digital or analog circuits have to process the output signals, which result from using the proposed circuit in different operation modes, and topology arrangements. We show the possible use of an array of Hamming neurons allowing the massively parallel processing of a precision alignment application. The Hamming distance comparator can be used as a standalone circuit for dedicated applications, or as an on-chip hardware accelerator for system-on-chip units.

References

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